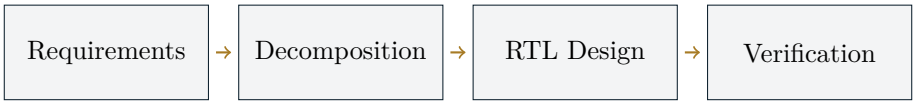
TargetDeLab

ENGINEERING & RESEARCH

Electronic Systems Design & Development

System-Level Decomposition • FPGA Programming
Custom Digital Architecture & IP Development

From complex system requirements to verifiable hardware implementations. TargetDeLab offers focused engineering collaboration, combining system-level architectural reasoning with practical FPGA and digital design execution.



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I System-Level Architecture & Decomposition

System-level decomposition is more than dividing a design into modules. It is the engineering process of converting objectives and constraints into an architecture whose components, interfaces and resource budgets can be implemented, integrated and verified.

Typical activities

- Interpret requirements, operating scenarios, interfaces and acceptance criteria.
- Decompose functions into subsystems, processing stages and control/data paths.
- Evaluate alternative architectures and hardware/software partitioning.
- Define inter-module contracts: interfaces, protocols, timing, buffering and error handling.
- Establish throughput, latency, clocking, memory, logic and power budgets where applicable.
- Identify integration risks and devise staged verification and prototype plans.

Potential deliverables

Architecture notes and block diagrams; subsystem specifications; interface definitions; data-flow and timing budgets; feasibility assessments; implementation plans; and verification strategies.

II FPGA Programming & RTL Development

FPGA programming is the primary implementation-oriented service. Assignments may range from a single well-defined RTL block to a coordinated set of hardware modules.

- VHDL/RTL module design, refactoring and integration.
- Finite-state machines, datapaths, counters, schedulers and control logic.
- Pipelined and parallel architectures for high-throughput processing.
- FIFOs, buffering, memory-access logic, arbitration and interface adaptation.
- Custom digital IP, protocol-handling blocks and algorithm-to-hardware translation.
- Simulation testbenches, debugging, timing review and resource optimization.

Target devices, toolchains, clock targets and deliverable formats are agreed per assignment. No universal device-family or performance guarantee is implied.

III Complementary Engineering Capabilities

Hardware/software co-design

Partition processing and control between programmable logic, embedded processors and host software. Evaluate communication overhead, synchronization, memory exchange and performance trade-offs.

Digital communications & data processing

Architectures for communication interfaces, protocol processing, streaming data paths, digital signal processing and high-rate data handling, subject to project requirements.

Embedded & electronic systems

Requirements-driven subsystem design, interface engineering, integration planning and technical evaluation for broader electronic products. PCB design, analog circuitry, fabrication and certification are considered only when explicitly scoped and resourced.

Design review & problem solving

Independent assessment of an existing FPGA or digital-system implementation, including architectural bottlenecks, RTL structure, simulation gaps, timing constraints and integration risks.

IV Typical Engagements

Focused RTL task	Design or correct a defined VHDL module, with testbench and documented interfaces.
Custom IP block	Implement a specialized controller, interface, processing block or hardware accelerator.
Architecture study	Translate a complex requirement into a subsystem architecture and feasibility plan.
Optimization review	Investigate timing, throughput, resource consumption or data-flow bottlenecks.
Integration support	Assist with module-level verification, interface compatibility and system bring-up planning.

Working principle: Define the problem precisely, identify measurable acceptance criteria, implement the smallest viable solution and verify the result against the agreed specification.

V From Requirement to Verified Deliverable

1. **Technical intake.** Review the problem statement, available documentation, constraints and existing design assets.
2. **Scope & feasibility.** Identify assumptions, dependencies, tools, target hardware, risks and expected outputs.
3. **Decomposition & design.** Define the functional architecture, interfaces, implementation strategy and verification plan.
4. **Implementation.** Develop the agreed RTL, models, testbenches or engineering documentation.
5. **Verification & delivery.** Provide evidence of testing, known limitations, integration guidance and agreed deliverables.

VI Engineering Background

The engineering capability described here draws on the professional work of **Dr. Napoleon V. Stefanopoulos**, whose background includes electrical engineering, telecommunications R&D, FPGA-based digital systems, hardware/software interaction, algorithm development and performance analysis.

He received a Diploma in Electrical Engineering and Computer Science from the National Technical University of Athens in 1995 and a Ph.D. in Telecommunications from the same institution in 1999. His work has included high-density FPGA prototypes, communications and protocol processing, digital architectures and the translation of analytical concepts into practical implementations.

This profile describes engineering expertise and potential services. Specific project availability, deliverables, licensing, confidentiality terms and commercial arrangements are determined separately for each engagement.

VII Discuss a Project

Have a difficult FPGA or electronic-system design task?

Provide a short technical description, target platform if known, available design files, performance constraints and desired deliverables. TargetDeLab can assess the scope and propose a suitable engineering approach.

Contact: Through the Contact section of TargetDeLab.com.